NEHRU COLLEGE OF ENGINEERING AND RESEARCH CENTRE

(Accredited by NAAC, Approved by AICTE New Delhi, Affiliated to APJKTU)

Pampady, Thiruvilwamala(PO), Thrissur(DT), Kerala 680 588

DEPARTMENT OF MECHATRONICS

LAB WORKBOOK

EC 234 LINEAR INTEGRATED CIRCUITS AND DIGITAL ELECTRONICS LABORATORY

VISION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2013
- Course offered: B.Tech Mechatronics Engineering
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

DEPARTMENT VISION

To develop professionally ethical and socially responsible Mechatronics engineers to serve the humanity through quality professional education.

DEPARTMENT MISSION

MD 1: The department is committed to impart the right blend of knowledge and quality education to create professionally ethical and socially responsible graduates.

MD 2: The department is committed to impart the awareness to meet the current challenges in technology.

MD 3: Establish state-of-the-art laboratories to promote practical knowledge of mechatronics to meet the needs of the society.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: Graduates shall have the ability to work in multidisciplinary environment with good professional and commitment.

PEO2: Graduates shall have the ability to solve the complex engineering problems by applying electrical, mechanical, electronics and computer knowledge and engage in lifelong learning in their profession.

PEO3: Graduates shall have the ability to lead and contribute in a team with entrepreneur skills, professional, social and ethical responsibilities.

PEO4: Graduates shall have ability to acquire scientific and engineering fundamentals necessary for higher studies and research.

PROGRAM OUTCOMES (PO'S)

Engineering Graduates will be able to:

PO 1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO'S)

PSO 1: Design and develop Mechatronics systems to solve the complex engineering problem by integrating electronics, mechanical and control systems.

PSO 2: Apply the engineering knowledge to conduct investigations of complex engineering problem related to instrumentation, control, automation, robotics and provide solutions.

COURSE OUTCOME

C215.1	Acquire the basic knowledge about Operational amplifiers and its applications.
C215.2	Demonstrate the working of adder and subtractor circuits using logic ICs.
C215.3	Design and set up different shift registers and counters
C215.4	Acquire knowledge to generate various waveforms using opamps
C215.5	Demonstrate different mathematical operations using opamp

CO VS PO'S AND PSO'S MAPPING

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO 1	PSO 2
C215.1	3	3	3.00	3					3			2	3	3
C215.2	3	3	3.00	3					3			2	3	3
C215.3	3	3	3.00	3					3			2	3	3
C215.4	3	3	3.00	3					3			2	3	3
C215.5	3	3	3.00	3					3			2	3	3
C 215	3.00	3.00	3.00	3.00					3.00	0.00	0.00	2.00	3.00	3.00

Note: H-Highly correlated=3, M-Medium correlated=2, L-Less correlated=1

PREPARATION FOR THE LABORATORY SESSION
GENERAL INSTRUCTIONS TO STUDENTS

1. Read carefully and understand the description of the experiment in the lab manual. You may go to the lab at an earlier date to look at the experimental facility and understand it better. Consult the appropriate references to be completely familiar with the concepts and hardware.

2. Make sure that your observation for previous week experiment is evaluated by the faculty member and your have transferred all the contents to your record before entering to the lab/workshop.

3. At the beginning of the class, if the faculty or the instructor finds that a student is not adequately prepared, they will be marked as absent and not be allowed to perform the experiment.

4. Bring necessary material needed (writing materials, graphs, calculators, etc.) to perform the required preliminary analysis. It is a good idea to do sample calculations and as much of the analysis as possible during the session. Faculty help will be available. Errors in the procedure may thus be easily detected and rectified.

5. Please actively participate in class and don't hesitate to ask questions. Please utilize the teaching assistants fully. To encourage you to be prepared and to read the lab manual before coming to the laboratory, unannounced questions may be asked at any time during the lab.

6. Carelessness in personal conduct or in handling equipment may result in serious injury to the individual or the equipment. Do not run near moving machinery/equipment's. Always be on the alert for strange sounds. Guard against entangling clothes in moving parts of machinery.

7. Students must follow the proper dress code inside the laboratory. To protect clothing from dirt, wear a lab coat. Long hair should be tied back. Shoes covering the whole foot will have to be worn.

8. In performing the experiments, please proceed carefully to minimize any water spills, especially on the electric circuits and wire.

9. Maintain silence, order and discipline inside the lab. Don't use cell phones inside the laboratory.

10. Any injury no matter how small must be reported to the instructor immediately.

11. Check with faculty members one week before the experiment to make sure that you have the handout for that experiment and all the apparatus.

AFTER THE LABORATORY SESSION

1. Clean up your work area.

2. Check with the technician before you leave.

3. Make sure you understand what kind of report is to be prepared and due submission of record is next lab class.

4. Do sample calculations and some preliminary work to verify that the experiment was successful

MAKE-UPS AND LATE WORK

Students must participate in all laboratory exercises as scheduled. They must obtain permission from the faculty member for absence, which would be granted only under justifiable circumstances. In such an event, a student must make arrangements for a make-up laboratory, which will be scheduled when the time is available after completing one cycle. Late submission will be awarded less mark for record and internals and zero in worst cases.

LABORATORY POLICIES

1. Food, beverages & mobile phones are not allowed in the laboratory at any time.

2. Do not sit or place anything on instrument benches.

3. Organizing laboratory experiments requires the help of laboratory technicians and staff. Be punctual.

SYLLABUS

Course code	Course Name	L-T-P - Credits	Year of Introduction
EC234	Linear Integrated Circuits and Digital Electronics Laboratory	0-0-3--1	2016

Prerequisite: EC212 Linear integrated circuits and digital electronics

Course Objectives

- To study various digital and linear integrated circuits used in simple system configuration

List of Exercises/Experiments : (10 experiments are mandatory)

1. Operational Amplifiers (IC741)-Characteristics
2. Square , triangular and ramp generation using op-amps
3. Log and Antilog amplifiers.
5. Astable and monostable multivibrators using op-amps
6. Active notch filter realization using op-amps
7. Wein bridges oscillator using OpAmp
8. OpAmp Integrator and Differentiator.
9. Code converter - Binary to gray and Gray to binary.
10. Adder and Subtractor Circuits using logic IC
11. Implementation of combinational logic circuits using MUX IC
12. Design and implementation of multiplexer and demultiplexer.
13. 3-bit synchronous counter design
14. Asynchronous counter design and Mod-n counter
15. Shift registers - SISO/SIPO & PISO/PIPO
16. Ring and Johnson Counters

List of major equipment

CRO, Function generator , Single power supply , Dual power supply, Digital multimeter, Ammeter ,Voltmeter.

Expected outcome .

On completion ,the students will be able to

1. Design simple circuits like amplifiers using OP-AMPs.
2. Design waveform Generating circuits.
3. Understand Digital concepts
4. Logically explain the concepts of combinational and sequential circuits.

Text Book:

1.RamakantA.Gayakward, Op-amps and Linear Integrated Circuits, IV edition, Pearson Education, 2003 / PHI.
2. D.RoyChoudhary, SheilB.Jani, Linear Integrated Circuits, II edition, New Age, 2003.
3. M. Morris Mano, Digital Logic and Computer Design, Prentice Hall of India, 2002

EXP NO	EXPERIMENT NAME	PAGE NO	MARK	SIGN
1	MEASUREMENT OF OP AMP PARAMETERS	8		
2	INTEGRATOR AND DIFFERENTIATOR	11		
3	SQUARE, TRIANGULAR AND RAMP GENERATOR	15		
4	ASTABLE AND MONOSTABLE MULTIVIBRATOR	19		
5	LOG AND ANTILOG AMPLIFIER	23		
6	ADDER AND SUBTRACTOR	26		
7	SHIFT REGISTERS	35		
8	ASYNCHRONOUS COUNTER	40		
9	RING AND JOHNSON COUNTER	45		
10	CODE CONVERTER	48		

FINAL VERIFICATION BY THE FACULTY
TOTAL MARKS:

INTERNAL EXAMINER **EXTERNAL EXAMINER**

EXPERIMENT NO : 1

MEASUREMENT OF OP AMP PARAMETERS

AIM:

To measure the following parameters of an Op-amp i.e, input bias current, input offset voltage, input offset current, CMRR and slew rate.

APPARATUS REQUIRED:

The following components and equipments are used to measure the op-amp parameters

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	4.7KΩ,100KΩ(2), 1MΩ, 100Ω(2),	Each one
5	Capacitor	0.01μF	1
6	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Input bias current I_B: It is defined as the average of the currents entering into the inverting and non-inverting terminals of an op-amp. $I_B = (I_{B1}+I_{B2})/2$. Typical value of input bias current is 80nA.

Input bias current I_O: It is defined as the algebraic difference between the currents entering into the inverting and non-inverting terminals of an op-amp. $I_O=|I_{B1}+I_{B2}|$. Typical value of input offset current is 20nA.

Input offset voltage: It is defined as the small voltage which is applied to overcome circuit imbalances due to which the output voltage is not zero for zero input voltage, i.e., voltage applied between the input terminals of an op-amp to nullify the output voltage. Typical value of input offset voltage is 2mV.

CMRR: It is the ratio of differential mode gain to common mode gain and is expressed in dB. CMRR=20 log (A_d/A_c) in dB.

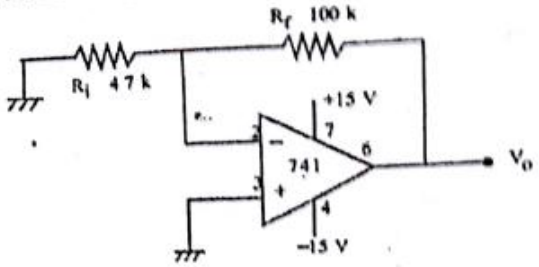
Slew rate: It is the rate of rise of output voltage. It is a measure of fastness of op-amp. It is expressed in v/μs.

PROCEDURE:

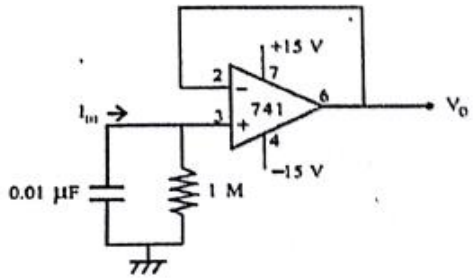
1. Set up the circuit to find the input offset voltage.
2. Measure the output voltage using the expression, $V_{io}=V_O R_i/(R_f + R_i)$; where V_O is the output voltage and V_{io} is the input offset voltage.

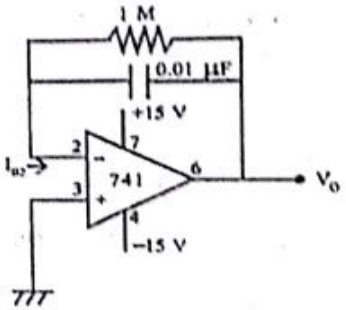
Circuit diagram

To measure input offset voltage

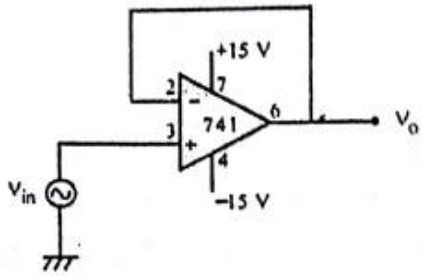


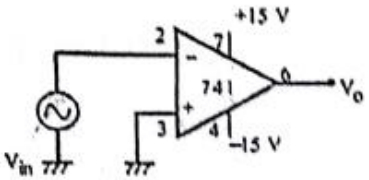
To measure input bias and input offset currents



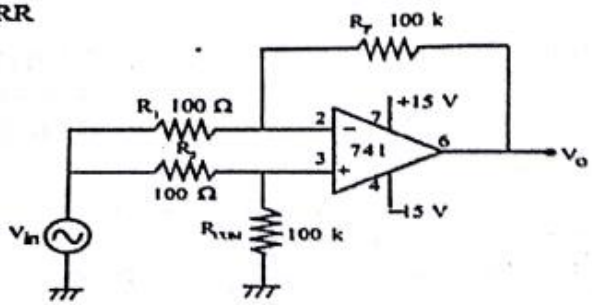


To measure slew rate





CMRR



3. Set up the circuits for measuring input bias current and input bias voltage
4. Measure the output voltage using the expressions $V_O = I_{b1}R$ and $V_O = I_{b2}R$.
5. Calculate I_{B1} and I_{B2} and measure the bias and offset currents using the expression $I_B = (I_{B1}+I_{B2})/2$and $I_O = |I_{B1} - I_{B2}|$. Where I_B is bias current, I_O is offset current.
6. Setup the circuit to calculate the slew rate. Give a square input of 1 V_{pp}, 1kHz. Vary the input frequency and observe the output. Note down the frequency at which the output gets disturbed. Calculate the slew rate using the expression $SR = (2\pi f V_m)/10^6$
7. Set up the circuits for finding CMRR and apply a dc signal of 0.5v to input and measure V_O. Calculate the CMRR using the expression $CMRR = V_i(R_f/R_i)/V_O$. Express the CMRR in dB using the expression 20 log(CMRR).

RESULT:

The various op-amp parameters were measured experimentally.

INFERENCE:

Input offset voltage = ……..mV
Input bias current = ……..A
Input offset current = ……..A
Slew rate = ……..V/μs.
CMRR = …….dB

EXPERIMENT NO : 2

INTEGRATOR AND DIFFERENTIATOR

AIM:

To design and set up integrator and differentiator circuits using op-amp and plot their frequency responses.

APPARATUS REQUIRED:

The following components and equipments are used to design and set up integrator and differentiator

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	150KΩ, 15KΩ(2), 5.6KΩ(2)	Each one
5	Capacitors	0.01uf, 0.1uf(2)	1
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by

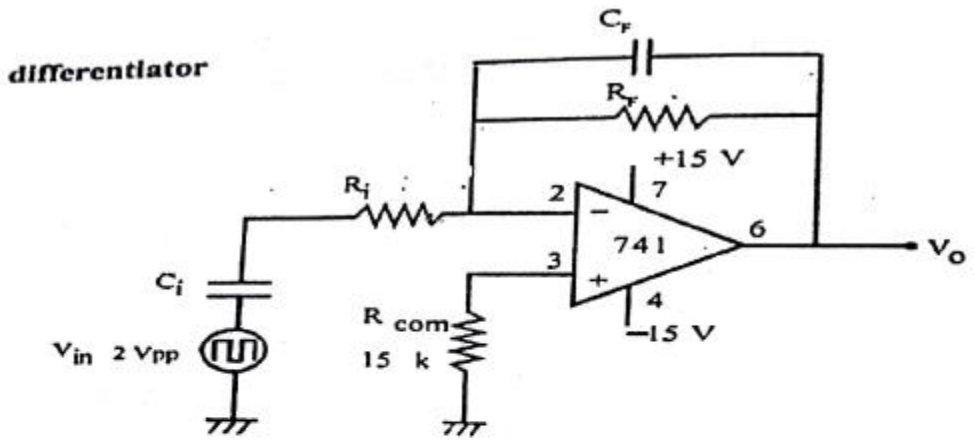
$$V_o = -1/R_1C_f \int_o^t Vidt$$

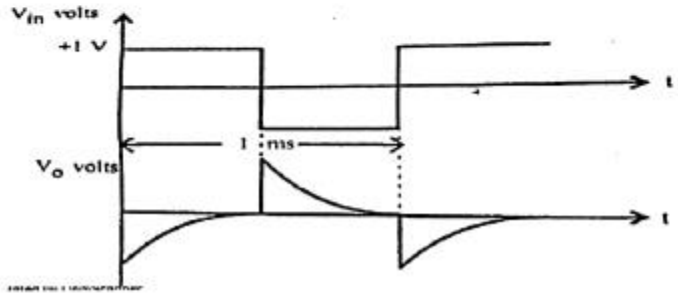
At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by

$$V_o = -RfC_1 \frac{dV_i}{dt}$$

The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.





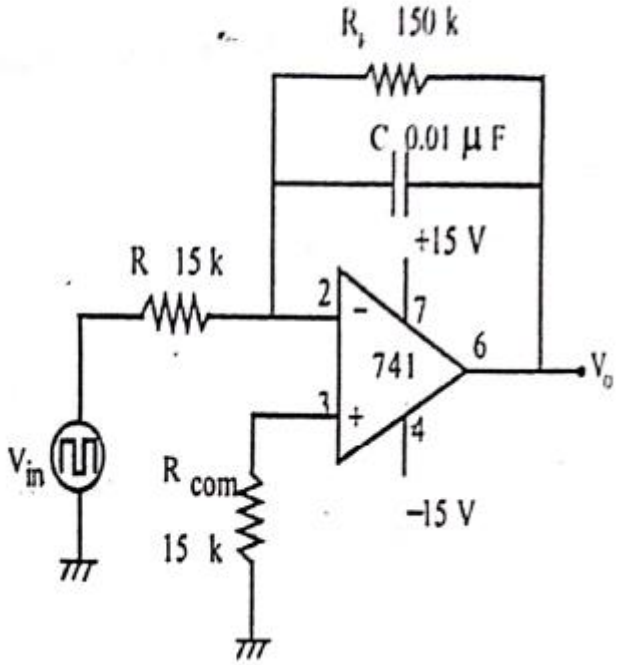
DESIGN:

INTEGRATOR:
Let input frequency be ,f= 1 kHz
$f = 1/ (2\pi RC)$
Take C=0.01 µf. Then R=15.9. Use 15k std.
Select $R_f = 10\ R = 10 * 15\ k = 150\ k$ so that break frequency is 100 Hz.
Select $R_{com} = 15k$

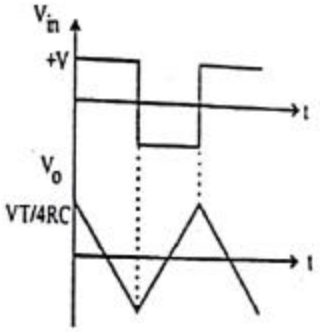
DIFFERENTIATOR:
Frequency at which gain become zero dB $f_a = 1/(2\pi R_f C_f) = 1$ kHz
Let C_f=0.01uF, Then R_f=15.9k. Use 15k std.
Let Gain limiting frequency, $f_b = 1/(2\pi R_f C_f) = 10 f_a = 10$kHz
Take C_i =0.01uF, Then R_i=1.59k. Use 1.5k std.
Select $R_{com} = 15k$

CIRCUIT DIAGRAM

INTEGRATOR



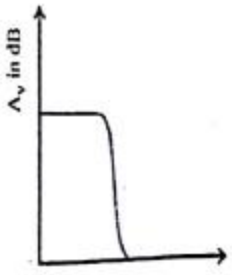
Waveforms



Tabular column

f in Hz	V_o	log (f)	A_v in dB

Frequency response



PROCEDURE:

INTEGRATOR:

1. Set up the integrator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response.

DIFFERENTIATOR:

1. Set up the differentiator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response

RESULT:

Integrator and differentiator circuits were studied and plotted their frequency responses.

INFERENCE:

Cut off frequency of low pass filter :.....Hz
Frequency at which gain become zero dB in differentiator:.....Hz
Gain limiting frequency of differentiator :.....Hz

EXPERIMENT NO : 3

SQUARE, TRIANGULAR AND RAMP GENERATOR

OBJECTIVE:

To set up and study a sawtooth and triangular wave form generator using Op-Amp for 1KHz frequency.

PRINCIPLE:

Triangular wave generator: This circuit uses two op-amps. One functions as a comparator and other as an integrator. Comparator compares the voltage at point P continuously with respect to the point voltage at the inverting input which is at zero volt. When voltage at P goes slightly above zero, the output of A will switch to negative saturation. Suppose the output of A is at positive saturation +Vsat, since this voltage is at the input of integrator, the output of A2 will be a negative going ramp. Thus one end of voltage divider R1 and R2 is at +Vsat and other end is at negative going ramp. At the time t=t1, when the negative going ramp attains the value of -Vramp, the effective voltage at P becomes slightly less than zero volt. This switches output of A1 from +Vsat to –Vsat level. The output of A2 increases in the positive direction. At the instant t=t2 , voltage at P becomes just above zero volt thereby switching the output of A from –Vsat to + Vsat . The cycle repeats and generates a triangular waveform. Frequency of triangular waveform f = (R1/4R2R3C) .Peak to peak amplitude of ramp voltage is 2(R2/R1) Vsat.

Saw tooth waveform generator: In sawtooth waveform generator the rise time is much higher than its fall time or vice -versa. The triangular waveform generator can be converted into a Sawtooth waveform generator by including a variable dc voltage into non inverting terminal of the integrator.This can be done by using a port. When the wiper of the port is at the centre ,the output will be a triangular wave since the duty cycle is 50%.If the wiper moves towards negative ,the rise time of Sawtooth becomes larger than fall time. If the wiper moves towards positive ,the fall time becomes larger than rise time. The Sawtooth waveform generators have wide applications in time base generators and pulse width modulation circuits.

MATERIALS AND METHODS:

The following components and equipments are used for conducting the experiment

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
3	CRO		1
3	Resistors	180Ω,12KΩ(pot),1KΩ(pot), 22KΩ(pot)	Each one
4	Capacitors	0.1uF	1
5	Op-amp	741	2
6	Bread board	-	1
7	Connecting wires	-	As required

The experimental procedure adopted is given below:

1. Set up the waveform generator circuit.
2. Obtain the output and note down the amplitude and frequency.
3. Set up the circuit of sawtooth wave generator.
4. Observe the output of both op-amps and note down the rise time and fall time.
5. Obtain the output by moving the wiper of port in both directions and observe the changes taking place in waveforms.

CIRCUIT DIAGRAMS:

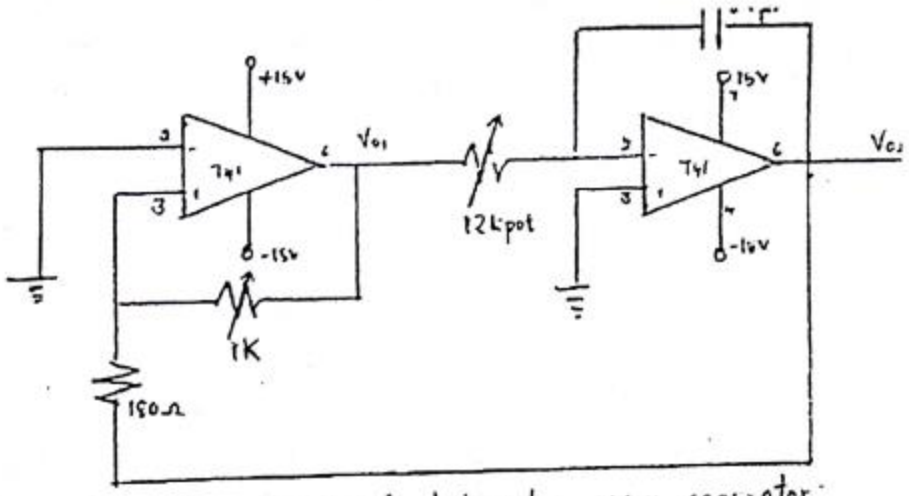


Fig (1): Circuit diagram of triangular wave generator

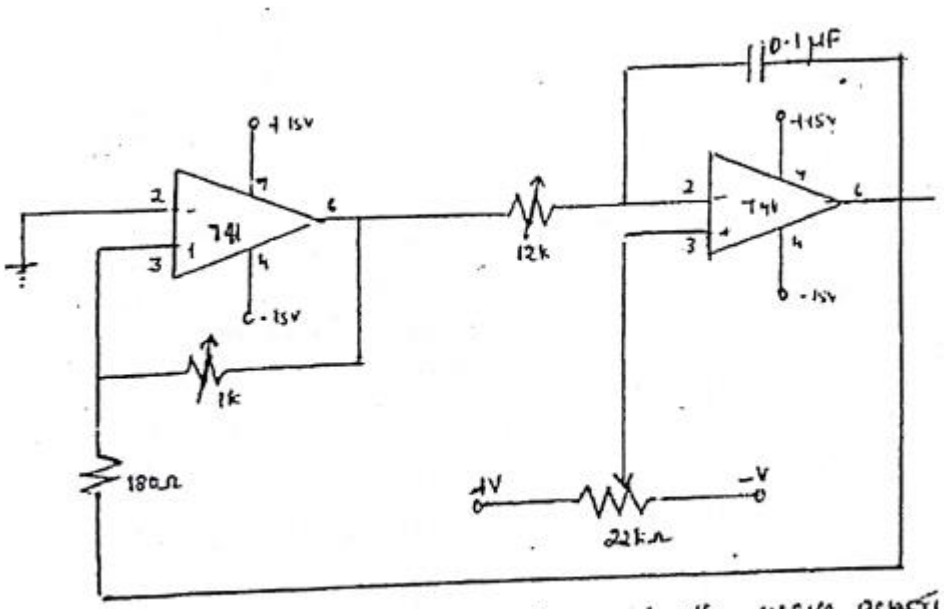


figure 2. Circuit diagram of sawtooth wave generator

DESIGN

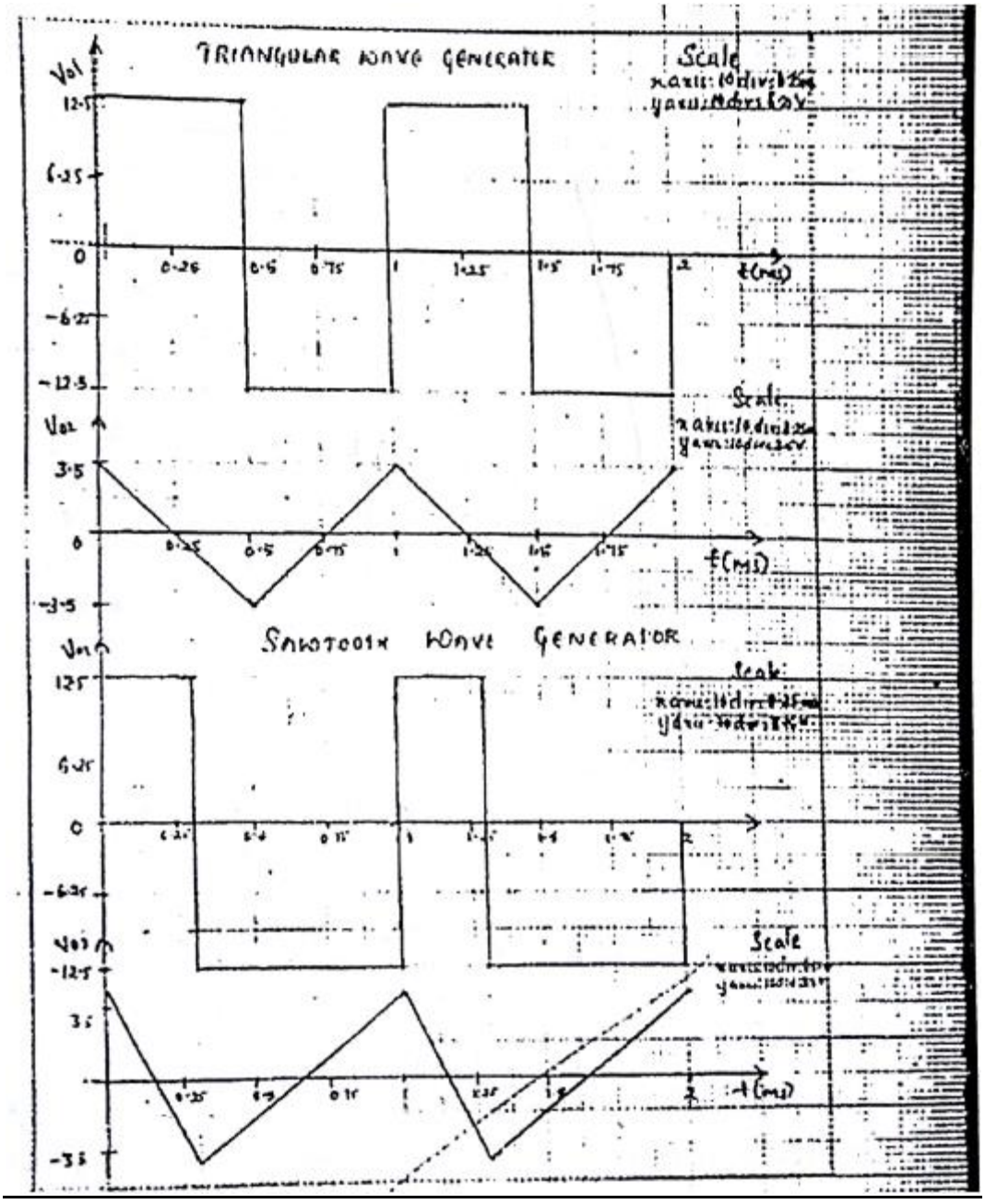
Triangular wave form generator

frequency,f =R1/(4*R2*R3*C)
Peak-peak output of ramp Vpp = 2R2/R1
Let the required Vpp = 5V and Vsat = 13 V
Assume R1 = 1Kohm then R2 = 180 ohm
Take C = 0.1 microF, so R3 = 13 K

Saw tooth wave form generator

frequency,f =R1/(4*R2*R3*C)
Peak-peak output of ramp Vpp = 2R2/R1
Let the required Vpp = 5V and Vsat = 13 V
Assume R1 = 1Kohm then R2 = 192 ohm Use 180 ohm standard
Take C = 0.1 microF, so R3 = 13 K Use 12K pot
Select R4 = 22 K

WAVEFORM



RESULTS AND DISCUSSION:-

CONCLUSION:-

EXPERIMENT NO : 4

ASTABLE & MONOSTABLE MULTIVIBRATOR

OBJECTIVE:

To design set up a astable and monostable multivibrators using op-amps for a frequency of 1kHz.

PRINCIPLE:

ASTABLE MULTIVIBRATOR: Astable multivibrators are capable of producing square wave for given frequency, amplitude and duty cycle. The output of an op-amp is forced to swing repetitively between positive saturation +Vsat and negative saturation –Vsat resulting in asquare wave output. This circuit is also called free running multivibrator or square wave generator. The output of the op-amp will be in positive saturation if differential input voltage is negative and vice versa. The differential voltage Vd = Vc -βVsat where β is the feedback factor. βVsat is the potential at non-inverting terminal of op-amp. Consider the instant at which Vo=+Vsat. Now the capacitor charges exponentially towards +Vsat through R. Automatically Vd increases and crosses zero. This happens when Vc changes to –Vsat. Now capacitor starts to discharge to zero and recharge towards –Vsat. Now Vd decreases and crosses zero. This happens when Vc=- βVsat. The moment Vd becomes negative again, output changes to +Vsat. This completes one cycle. The time period T of the square wave is T= 2RCln(1+β)/(1-β).If β is made ½, T= 2.2RC. Astable multivibrator is particularly useful for the generation of frequency in the audio frequency range. Higher frequencies are limited by the delay time and slew rate of the op-amp.

MONOSTABLE MULTIVIBRATOR: A Monostable Multivibrator, often called a one-shot Multivibrator. It ha a stable state and and a quasi stable state. The circuit remains in stable state until triggering signal causes a transition to quasi stable state. After a time interval, it returns to the stable state. So a single pulse of predetermined duration can be generated using this circuit. Consider the instant at which the output Vo=+Vsat. Now the diode D1 clamps the capacitor voltage Vc at 0.7V. feedback voltage available at non inverting terminal is +βVsat. When the negative going trigger is applied such that potential at non inverting terminal becomes less than 0.7 V , the output switches to –Vsat. Now the capacitor charges through R towards –Vsat, because the diode becomes reverse biased. When the capacitor voltage become more negative than –Vsat, the comparator switches back to +Vsat, and the capacitor C starts charging to +Vsat through R until Vc reaches 0.7.

MATERIALS AND METHODS:

The following components and equipments are used for conducting the experiment

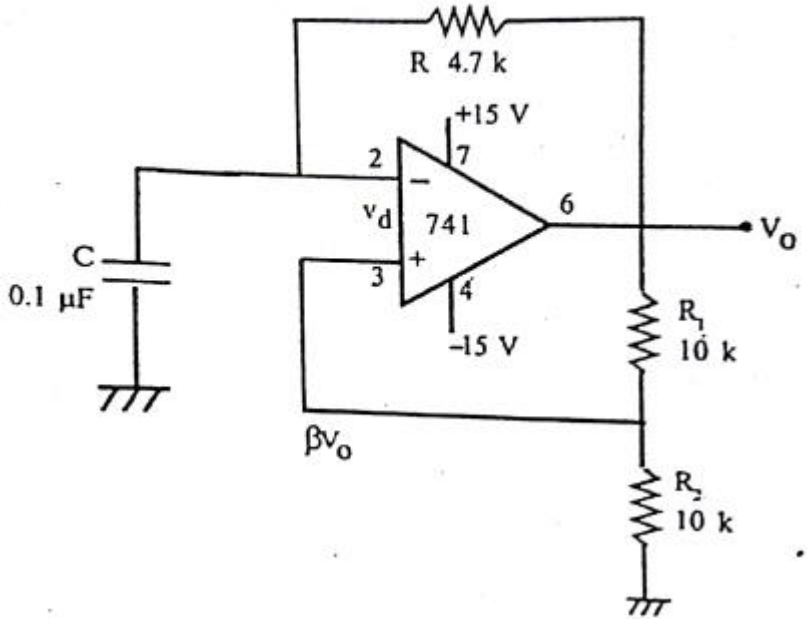
S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Functiongenerator	1MHz	1
3	CRO		1
4	Resistors	10KΩ(2),15KΩ,4.7KΩ,8.2K	Each one
5	Capacitors	0.1uF, 0.01uF(2)	Each One
6	diode	IN 4007	2
7	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

The experimental Procedure adopted is given below:

1. Verify the conditions of op-amp.
2. Set up the circuit astable multivibrator and observe the output waveform. Note down their frequencies and amplitudes.
3. Set up the circuit monostable multivibrator and feed 6Vpp,300Hz pulse at the trigger input and observe the output waveform. Note down their frequencies and amplitudes.

CIRCUIT DIAGRAMS:

ASTABLE MULTIVIBRATOR:



DESIGN:

Required period of oscillation T = 1 ms with duty cycle 50 %.

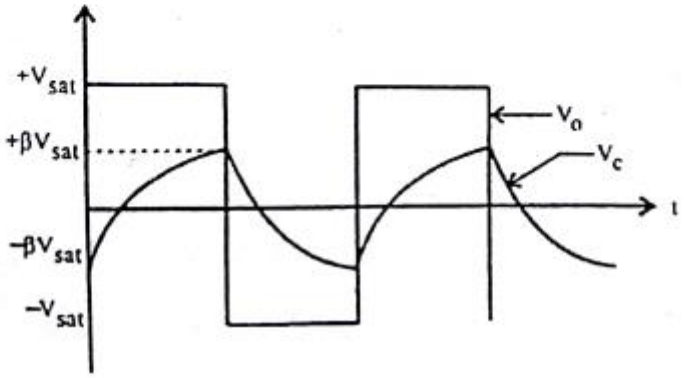
Time period $T = T_1 + T_2 = 2RC \ln(1 + \beta)/(1 - \beta)$

where β, the feedback factor $= R_2/(R_1 + R_2)$

Take $\beta = 0.5$ and $R_2 = 10$ k. Then $R_1 = 10$ k.

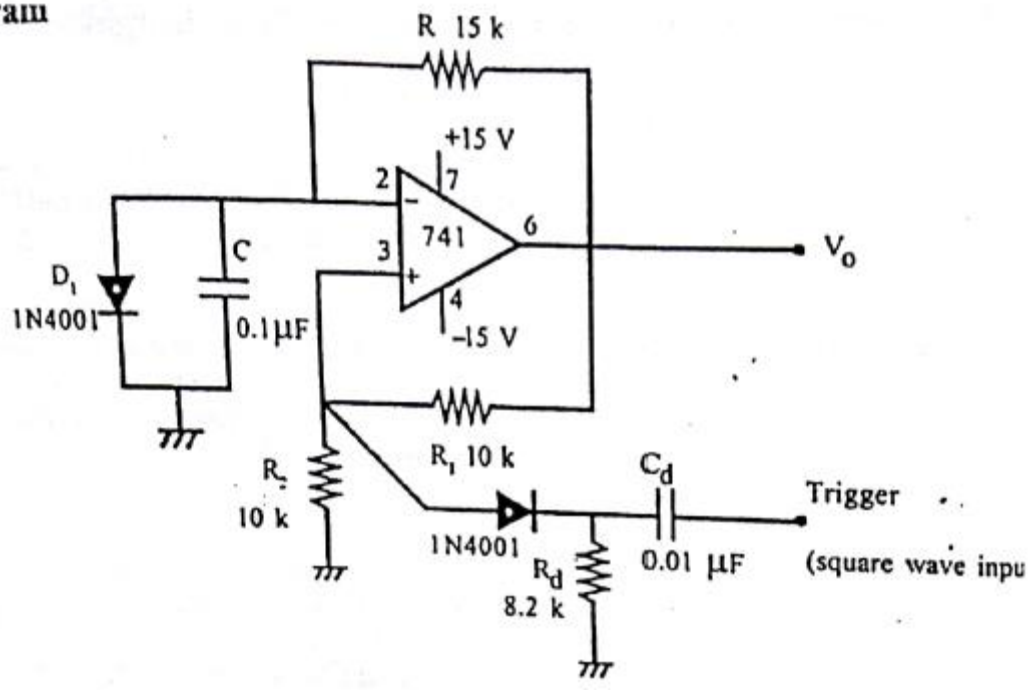
When $\beta = 0.5$, $T = 2.2\ RC$.

Let C be 0.1 μF. Then R = 4.7 k.



MONOSTABLE MULTIVIBRATOR:

ram



Design We have, $T = RC \ln[1/(1-\beta)]$. Let $\beta = 0.5$. Then $T = 0.69RC$

Take T = 1 ms and C = 0.1 μF. Then R = 14.5 k. Use 15 k std.

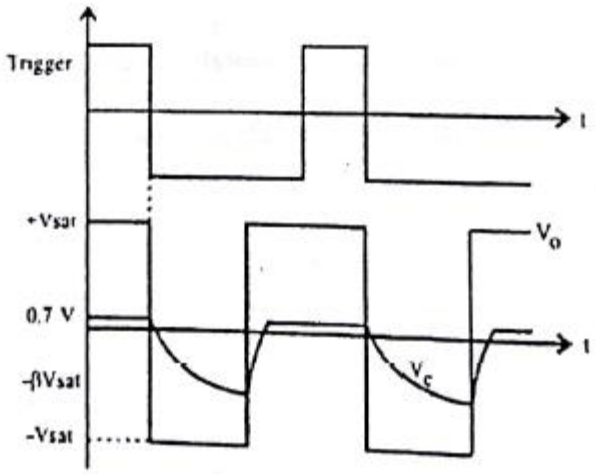
Since $\beta = R_2/(R_1 + R_2)$, $R_1 = R_2 = 10$ k.

Design of differentiating circuit: $R_dC_d < 0.016T_t$.

Take trigger time period $T_t = 5$ ms and $C_d = 0.01$ μF.

Then $R_d = 8.2$ k.

Waveforms



RESULT AND DISCUSSION:

CONCLUSION:

EXPERIMENT NO : 5

LOG & ANTI LOG AMPLIFIER

OBJECTIVE:

To understand the behavior of logarithmic and antilogarithmic amplifiers.

PRINCIPLE:

Log amplifiers are widely used for analog signal compression applications. When a diode used in the feedback loop of an operational amplifier is forward biased by a constant current of magnitude V_i /R then it develops a potential

$$V_D = V_T \ln\left(\frac{v_i}{RI_o}\right)$$

across the diode. Note that the input voltage and diode voltage are related in a logarithmic fashion. If we take the diode voltage as an output voltage then the input and output will be related in a logarithmic fashion. The base emitter junction of a bipolar junction transistor can be used as diode when collector and base are shorted. So a transistor can also be used in the feedback loop of an op-amp. Antilog is inverse operation of log operation so; antilog amplifiers can be designed by reversing the arrangement of diodes and resistors in the log amplifiers. It is important to note that a single polarity of current can only forward bias the diode. That means the log operation or antilog operation is single quadrant operation.

MATERIALS AND METHODS:

The following components and equipments are used for log and antilog amplifiers

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	100KΩ	2
5	Multimeter		1
6	Diode	IN 4007	2
7	Op-amp	IC 741	2
8	Bread board	-	1
9	Connecting wires	-	As required

The experimental Procedure adopted is given below:

Log amplifier:

1. Set up the circuit for log amplifier using diode and transistor.
2. Set the input voltage to 1V.and see the voltage across the diode and voltage across the output terminal. Note the negative sign.
4. Increase the input voltage in the step of 1V up to 20V.

5. Plot the characteristics of input voltage and output voltage.
6. Compare the characteristics of diode based log amplifier with that of transistor based log amplifier.
7. Reverse the polarity of the diode and see the effect for positive input voltage.

Anti log amplifier:

1. Set up the circuit for antilog amplifier using diode. Set the input voltage to 100mV.
2. See the voltage across the Resistor. Note the negative sign.
3. Increase the input voltage in the step of 50mV up to 500mV.
4. Plot the characteristics of input voltage and output voltage.
5. Reverse the polarity of the diode and see the effect for positive input voltage.

Log-anti log amplifier:

1Set up the circuit for log-antilog amplifier
2 Set the input voltage to 1V.See the voltage across the output resistor.
3 Increase the input voltage in the step of 1V up to 20V.
4 Note the output voltage for all the input voltages.
5 Please get confused why the output is not the exact replica of input.
6 Reverse the polarity of diode in the antilog amplifier of fig 4.
7Again set the input to 1V.
8 See the output and be angry with the output.
9 Increase the input from 1V and see the output.

CIRCUIT DIAGRAMS:

Log Amplifier using Diode

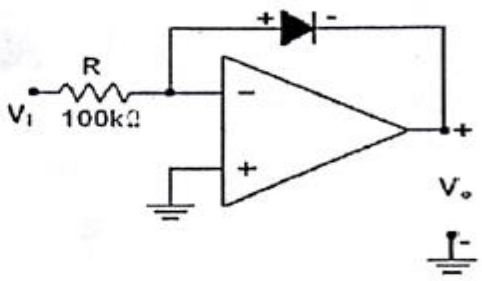


Fig 1

Log Amplifier Using a BJT

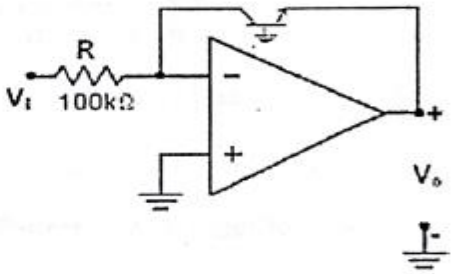


Fig 2

Anti-log Amplifier

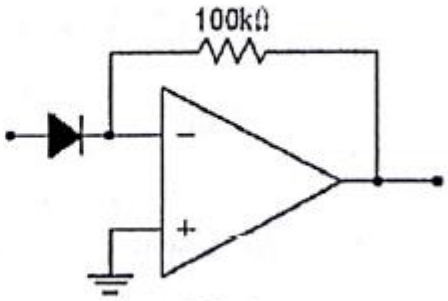


Fig 3

Log - Antilog Amplifier

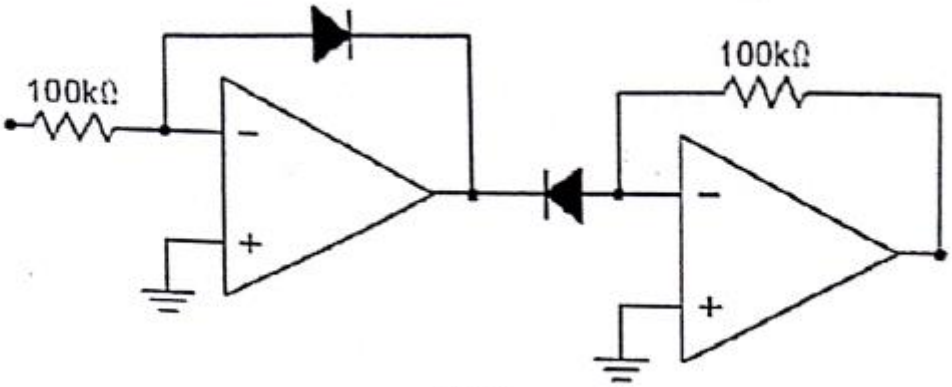


Fig 4

RESULT AND DISCUSSION:

CONCLUSION:

EXPERIMENT NO : 6

ADDER AND SUBTRACTOR

HALF ADDER AND FULL ADDER

AIM:

To design and setup Half adder and Full adder using

a) XOR and NAND gates.
b) NAND gates only

PRINCIPLE:

A combinational circuit that performs the addition of two bits is called a half adder. One that performs the addition of three bits (two bits and a previous carry) is a full adder.

HALF ADDER: $s = x'y + xy' = x \ominus y$

$c = xy$

FULL ADDER: $s = x'y'z + x'yz' + xy'z' + xyz = x \ominus y \ominus z$

$c = xy + xz + yz = (x \ominus y)z + xy$

PROCEDURE:

1. Test all the components and IC trainer packages using a digital IC tester.
2. Assure whether all the connection wires are in good condition by testing for the continuity using multimeter or a trainer kit. Continuity of wires can be tested using trainer kit by shorting a 5v supply in trainer kit to an LED. If wires are in good condition LED will Glow.
3. Verify the dual in line pin out of the IC before feeding the input.
4. Connect the circuit as given in the circuit diagram.
5. Verify the truth table of the circuit.

FULL ADDER

DESIGN

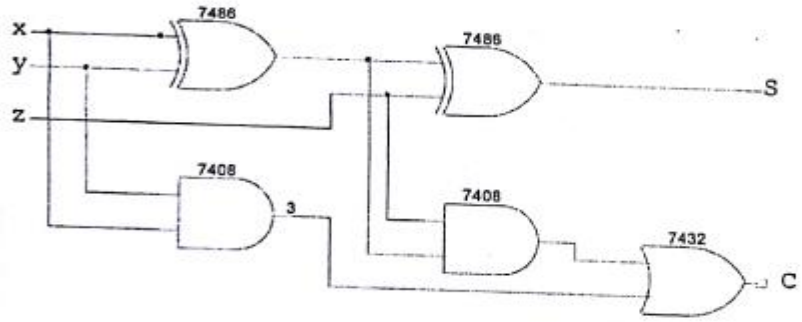
Truth Table

Input			Output	
x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

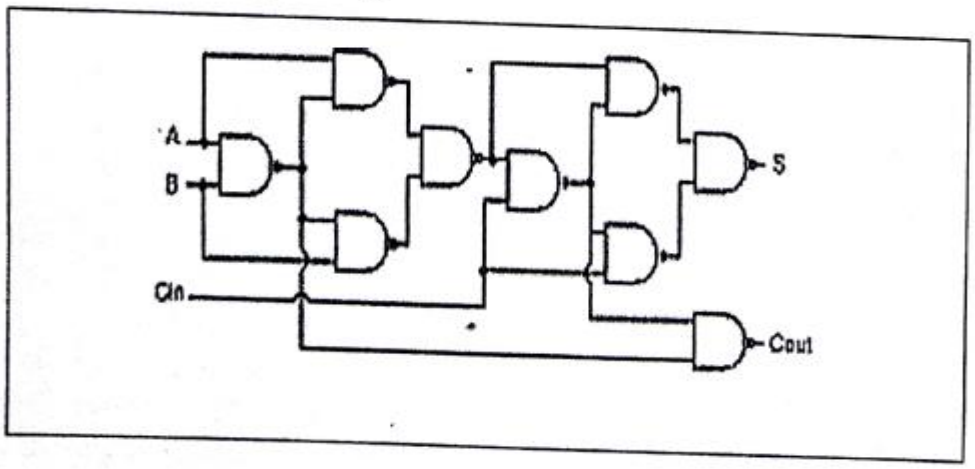
$s = x'y'z + x'yz' + xy'z' + xyz = x \ominus y \ominus z$

$c = xy + xz + yz = (x \ominus y)z + xy$
$= (((x \ominus y)z)' \cdot (xy)')'$

Full Adder using XOR and basic gates



Full Adder using NAND gates only



HALF ADDER

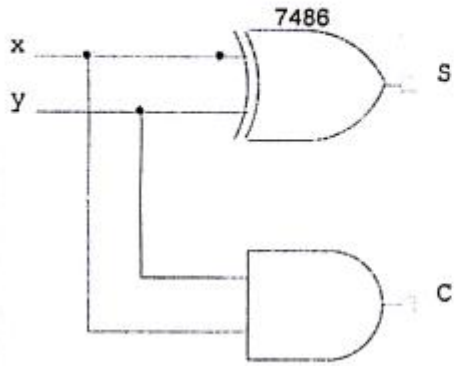
DESIGN

TRUTH TABLE

Input		Output	
x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

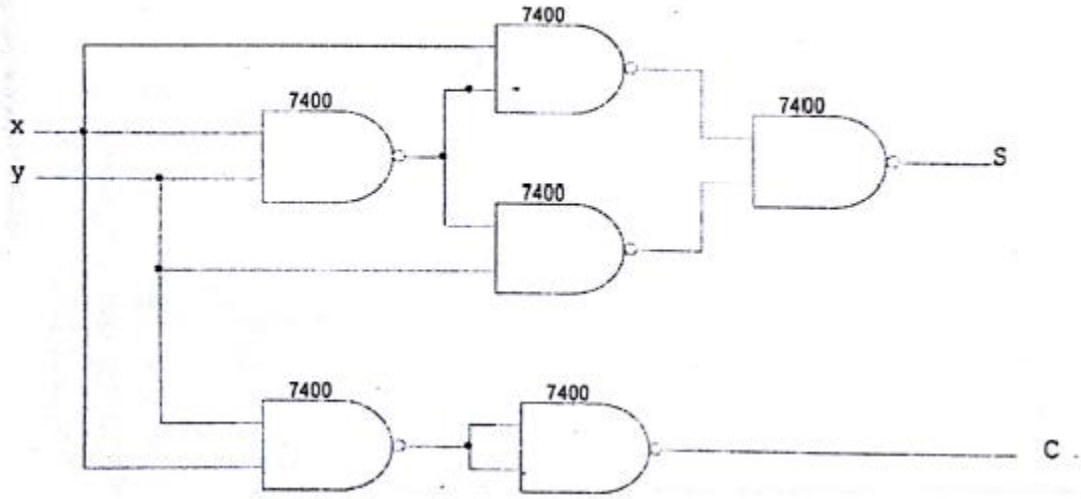
$s = x'y + xy' = x \oplus y$ = x Ex Or y

HALF ADDER USING XOR & AND GATES



7408

HALF ADDER USING NAND GATES ONLY



RESULT:

The half adder and full adder were designed and implemented using logic gates.

INFERENCE:

In half adder only 2 bits can be used where as in full adder 3 bit data can be used.

HALF SUBTRACTOR AND FULL SUBTRACTOR

AIM:

To design and setup Half Subtractor & Full Subtractor using

a) XOR and basic gates.
b) NAND gates only

APPARATUS REQUIRED:

1. IC 7408, 7486 , 7432 , 7404
2. IC Trainer Kit

PRINCIPLE:

A combinational circuit that performs the subtraction of two bits is called a half subtractor. One that performs the subtraction of three bits (two bits and a borrow) is a full subtractor.

HALF SUBTRACTOR: $D = x'y + xy' = x \ominus y$

$c = x'y$

FULL SUBTRACTOR: $D = x'y'z + x'yz' + xy'z' + xyz = x \ominus y \ominus z$

$c = (x \ominus y)'z + x'y$

PROCEDURE:

1. Test all the components and IC trainer packages using a digital IC tester.
2. Assure whether all the connection wires are in good condition by testing for the continuity using multimeter or a trainer kit. Continuity of wires can be tested using trainer kit by shorting a 5v supply in trainer kit to an LED. If wires are in good condition LED will Glow.
3. Verify the dual in line pin out of the IC before feeding the input.
4. Connect the circuit as given in the circuit diagram.
5. Verify the truth table of the circuit.

HALF SUBTRACTOR

DESIGN

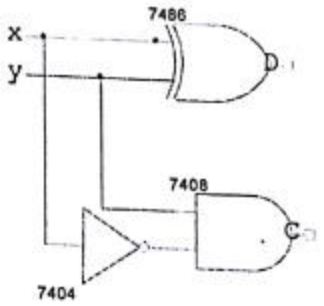
Truth Table

Input		Output	
x	y	D	c
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

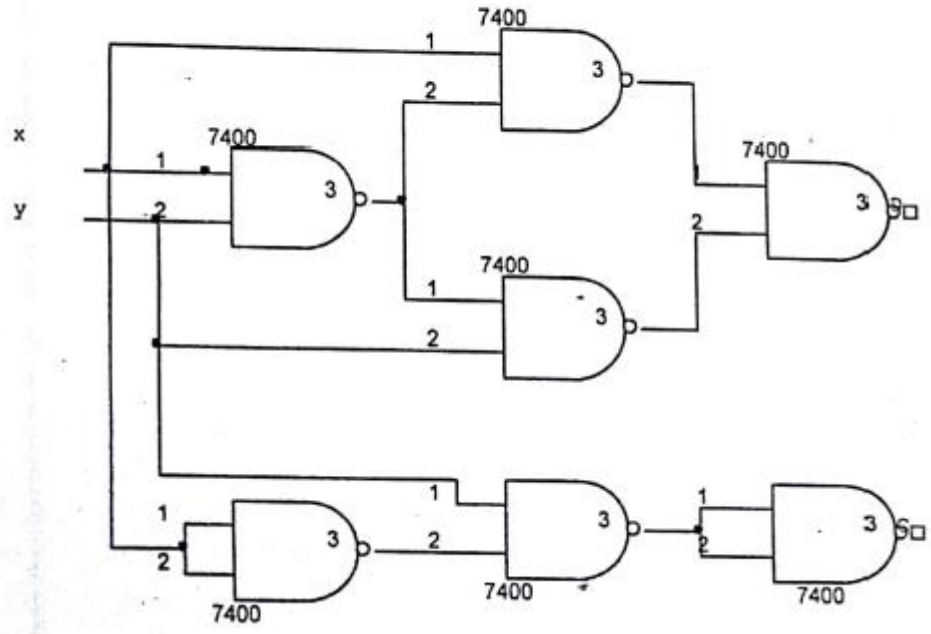
$D = x'y + xy' = x \ominus y$

$c = x'y$

Half Subtractor using XOR and basic gates



Half Subtractor using NAND gates only



FULL SUBTRACTOR

DESIGN

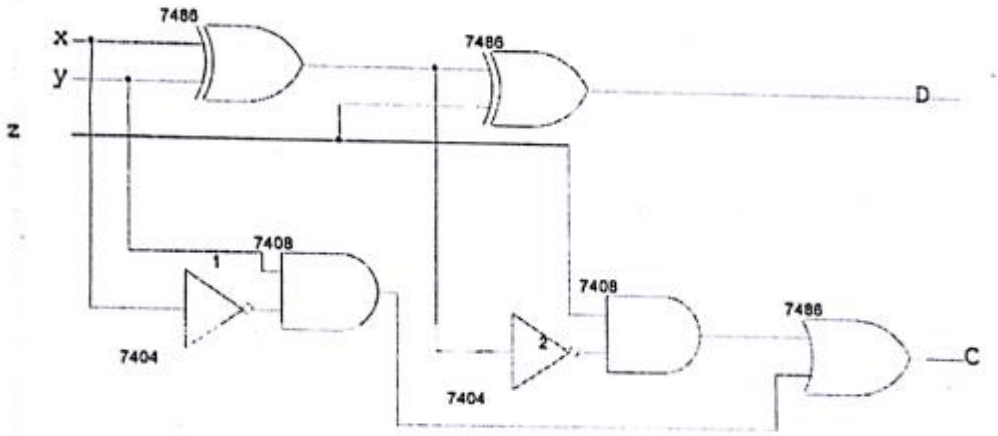
Truth Table

Input			Output	
x	y	z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

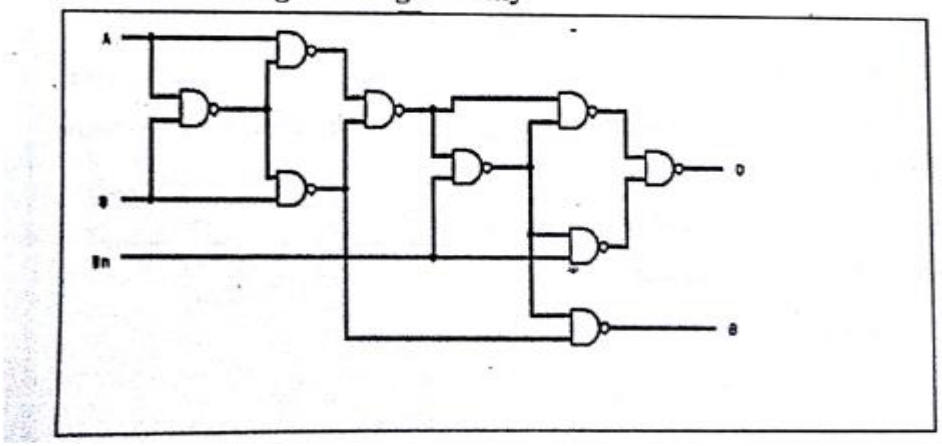
$D = x'y'z + x'yz' + xy'z' + xyz = x \ominus y \ominus z$

$B = (x \ominus y)'z + x'y$
$= (((x \ominus y)'z)' . (x'y)')'$

Full Subtractor using XOR and basic gates



Full Subtractor using NAND gates only



RESULT:

The half subtractor and full subtractor were designed and implemented using logic gates.

INFERENCE:

In half substractor only 2 bit data can be subtracted but in full substractor 3 bit data can be subtracted.

EXPERIMENT NO : 7

SHIFT REGISTERS

AIM:

To implement the following shift registers using flipflops:

(i) Serial In Serial Out (SISO)
(ii) Serial In Parallel Out (SIPO)
(iii) Parallel In Serial Out (PISO)
(iv) Parallel In Parallel Out (PIPO)

APPARATUS REQUIRED:

1. IC Trainer Kit
2. IC 7474,7432,7404

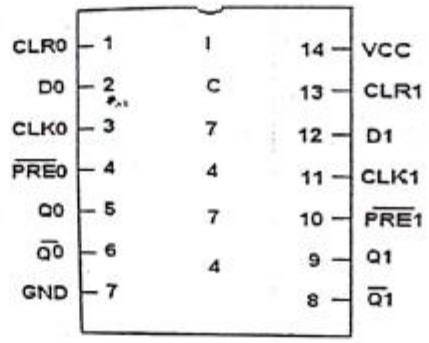
PRINCIPLE:

A register is a group of flipflops used to store digital data. A shift register is a memory in which information is shifted one position at a time when one clock pulse is applied. The data can be shifted in either direction ie towards the right (right shift register) or towards the left (left shift register). Data can be input to a shift register either in serial or parallel. Similarly, data can be output either in serial or parallel. Thus, there can be four different configurations of shift registers depending on the way in which data is entered or outputted. These are (i) SISO (ii) SIPO (iii) PISO (iv) PIPO.

Serial input shift register:
Set up the circuit as shown in the circuit diagram. Clear all the flipflops by setting CLEAR to logic 0. After that, set CLEAR to logic 1. Feed a 3 bit binary number to the serial input starting from LSB. Three clock pulses are required to shift the 3 bits into the shift register. The parallel outputs are available at $Q_2Q_1Q_0$ for the SIPO. To see the output at the serial output for the SISO, further clock pulses are applied to shift the bits to the right.

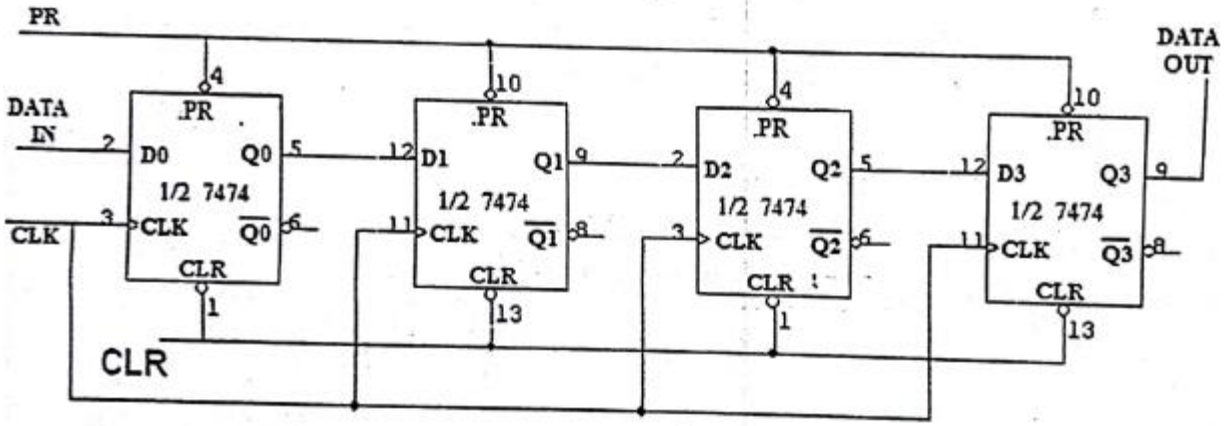
Parallel input shift register:
Set up the circuit as shown in the circuit diagram. Clear all the flipflops by setting CLEAR to logic 0. After that set CLEAR to logic 1. For the PIPO, binary data is fed in through D_2, D_1, D_0 and observed at $Q_2Q_1Q_0$. For the PISO, the control input Load/Shift is first connected to logic 1. The binary input is fed in through D_2, D_1, D_0. Then the control input is set to logic 0. On application of clock pulses the data in the shift register is shifted right and observed at the serial output.

PIN DIAGRAM – IC 7474



(i) SERIAL IN SERIAL OUT (SISO) SHIFT REGISTER

CIRCUIT DIAGRAM

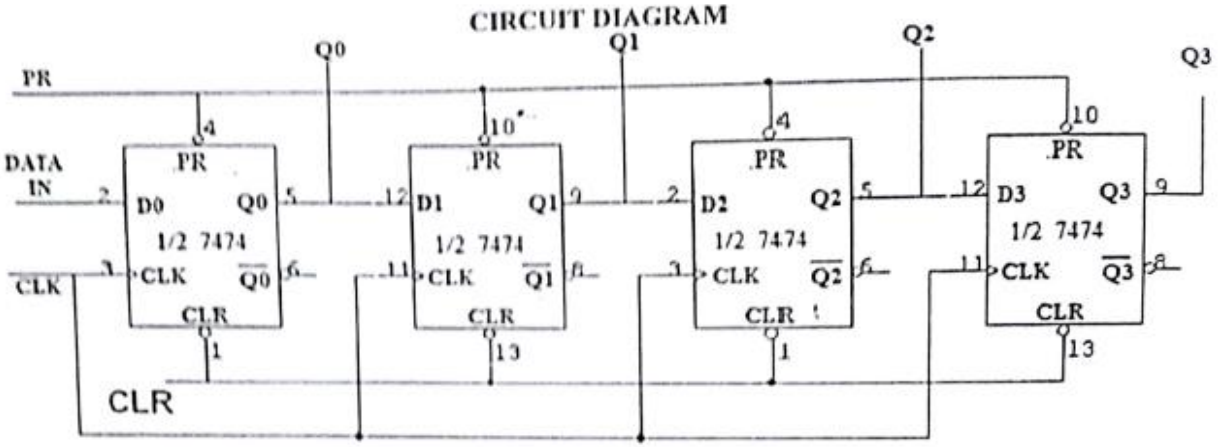


TRUTH TABLE

CLK	DATA IN	DATA OUT
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

(ii) SERIAL IN PARALLEL OUT (SIPO) SHIFT REGISTER

CIRCUIT DIAGRAM

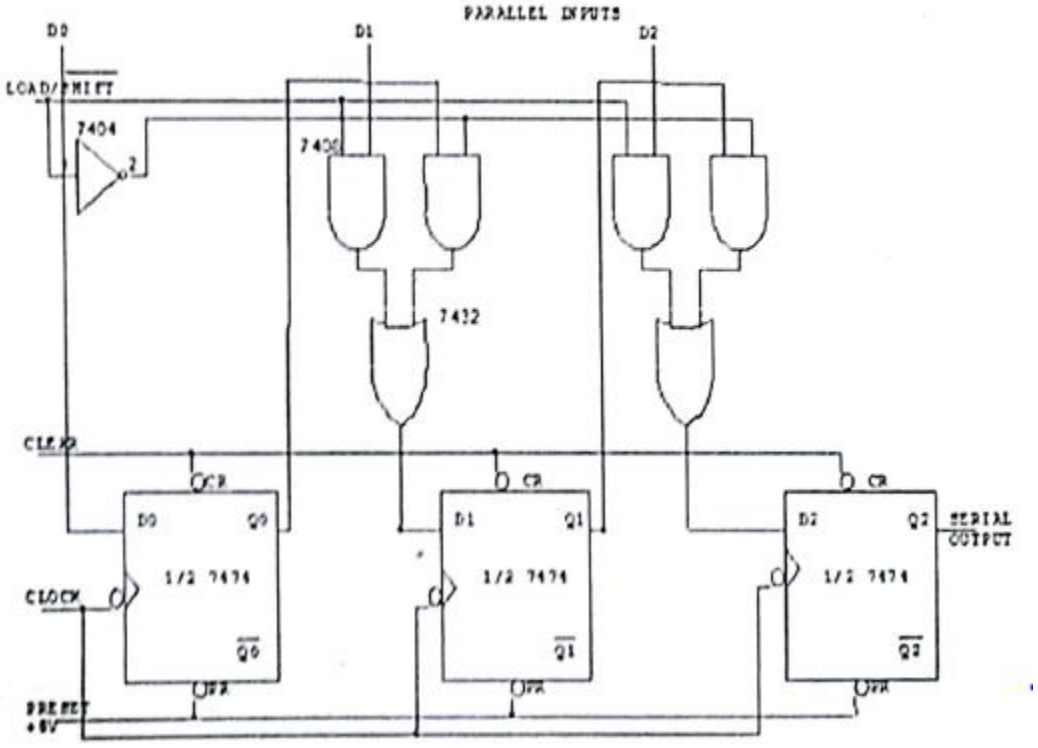


TRUTH TABLE:

CLK	DATA	OUTPUT			
		Q_0	Q_1	Q_2	Q_3
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	1	1	0	0	1

(iii) PARALLEL IN SERIAL OUT SHIFT (PISO) REGISTER

CIRCUIT DIAGRAM



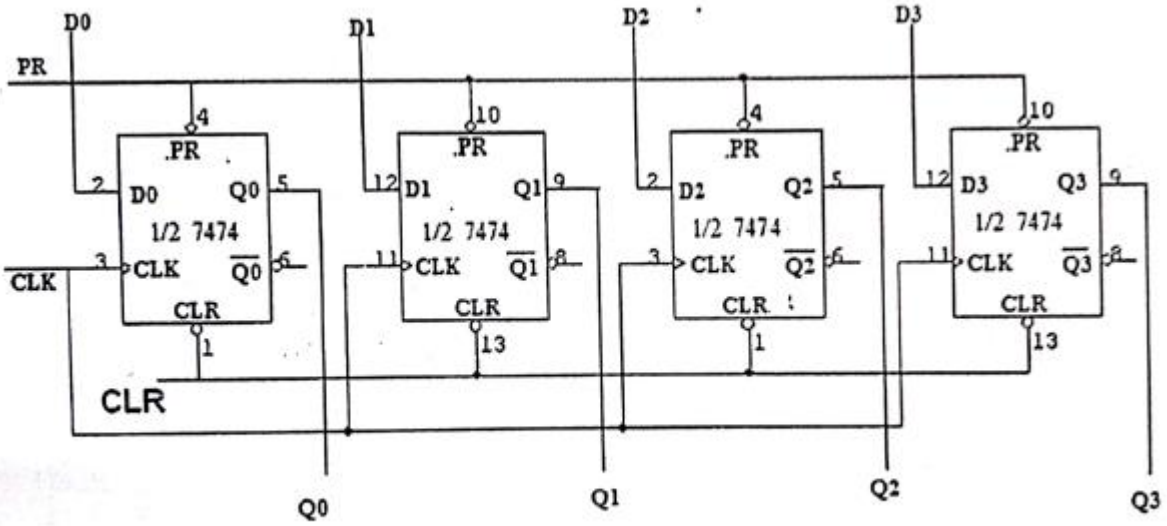
TRUTH TABLE

CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

(iv) PARALLEL IN PARALLEL OUT (PIPO) SHIFT REGISTER

CIRCUIT DIAGRAM

PARALLEL INPUTS



PARALLEL OUTPUTS

TRUTH TABLE:

CLK	DATA INPUT				OUTPUT			
	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

PROCEDURE:

1. Test all the components and IC trainer packages using a digital IC tester.
2. Assure whether all the connection wires are in good condition by testing for the continuity using multimeter or a trainer kit. Continuity of wires can be tested using trainer kit by shorting a 5v supply in trainer kit to an LED. If wires are in good condition LED will Glow.
3. Verify the dual in line pin out of the IC before feeding the input.
4. Connect the circuit as given in the circuit diagram.
5. Verify the truth table of the circuit.

RESULT:

Thus the Serial in serial out, Serial in parallel out, Parallel in serial out and Parallel in parallel out shift registers were implemented using IC 7474.

INFERENCE:

Verified functionality of shift registers and identified their unique features along with area of application.

EXPERIMENT NO : 8

ASYNCHRONOUS COUNTER

AIM:

To construct and verify the operation of a

(i) 4 bit ripple counter

(ii) MOD 10 ripple counter

(iii) MOD 12 ripple counter.

APPARATUS REQUIRED:

IC 7476, 7400, Digital IC Trainer kit

THEORY:

A register that goes through a prescribed sequence of states upon the application of an input pulse is called a counter. The input pulses may be clock pulses or may originate from some external source and may occur at fixed intervals of time or at random.

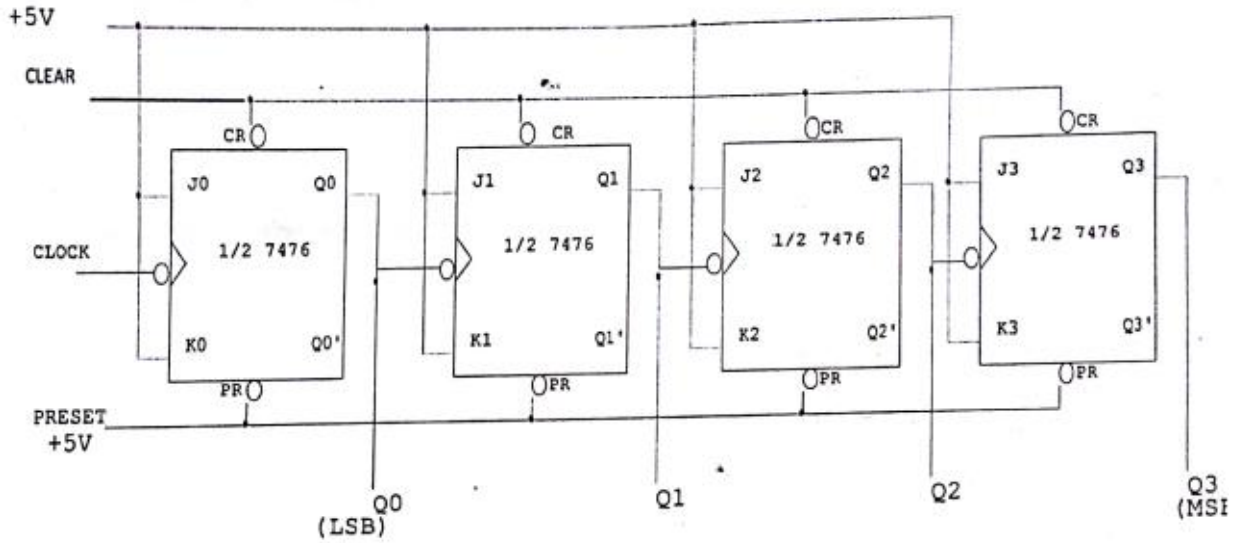
The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follows the binary number sequence is called a binary counter. An n bit binary counter consists of n flipflops and can count in binary from 0 to 2^{n-1}. The number of unique states that a counter can count is called the modulus of a counter. A MOD-N counter counts N unique states for eg from 0 to N-1.

Counters are of two main kinds: ripple (or asynchronous) counters and synchronous counters. In a ripple counter, the flipflop output transition serves as a source of triggering other flipflops ie the clock inputs of all the flipflops are not triggered by the common clock.

PROCEDURE:

1. Test all the ICs used in the circuit.
2. Set up the circuit for the 4 bit ripple counter
3. Clear the $Q_3Q_2Q_1Q_0$ outputs by connecting clear pins to logic 0.After that, connect the clear pins to +5V
4. Apply clock pulses and observe the counter outputs. The counter counts from 0000 to 1111.
5. Repeat the above steps for the MOD 10 counter. The counter counts from 0000 to 1001.
6. Repeat the above steps for the MOD 12 counter. The counter counts from 0000 to 1011.

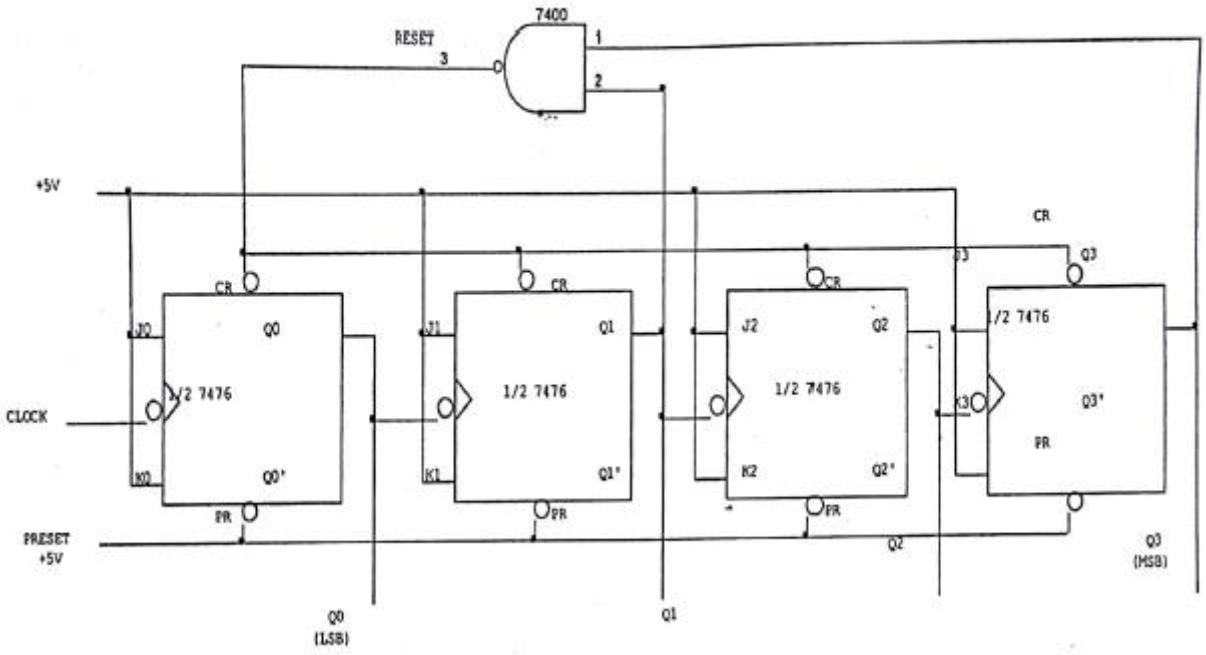
4 BIT RIPPLE COUNTER (UP COUNTER)



TRUTH TABLE:

CLK	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

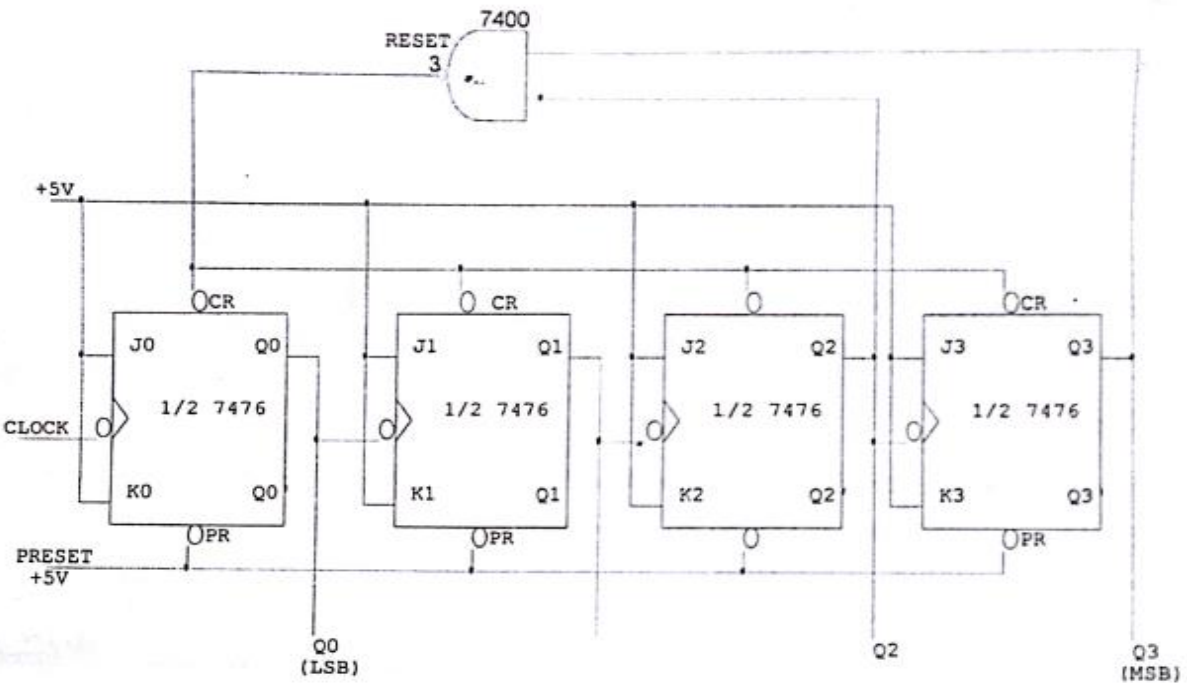
MOD 10 COUNTER



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

MOD 12 COUNTER



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

RESULT:

(i) 4 bit ripple counter

(ii) MOD 10 ripple counter

(iii) MOD 12 ripple counter were constructed and the operation verified.

INFERENCE:

Thus the 4 bit ripple counter, mod 10/ mod 12 ripple counters was implemented and the truth table was verified.

EXPERIMENT NO : 9

RING AND JOHNSON COUNTER

AIM

To design and set up four bit Johnson and ring counter using JK FF

COMPONENTS REQUIRED

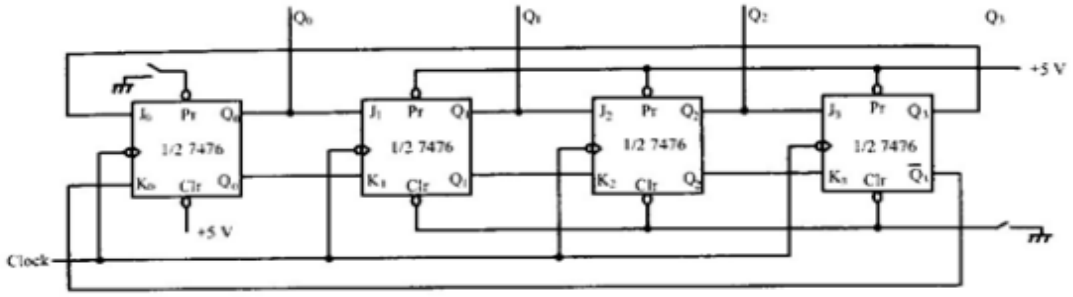
Digital IC trainer kit, IC 7476

PRINCIPLE

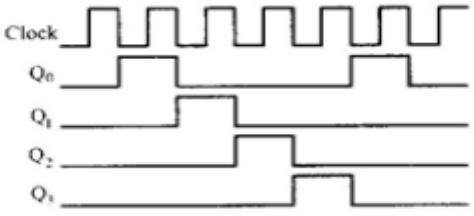
Ring counter and Johnson counters are basically shift registers

Ring counter

It is made by connecting Q&Q' output of one JK FF to J&K input of next FF respectively. The output of final FF is connected to the input of first FF. To start the counter the first FF is set by using preset facility and the remaining FF are reset input. When the clock arrives the set condition continues to shift around the ring



Waveforms for ring counter



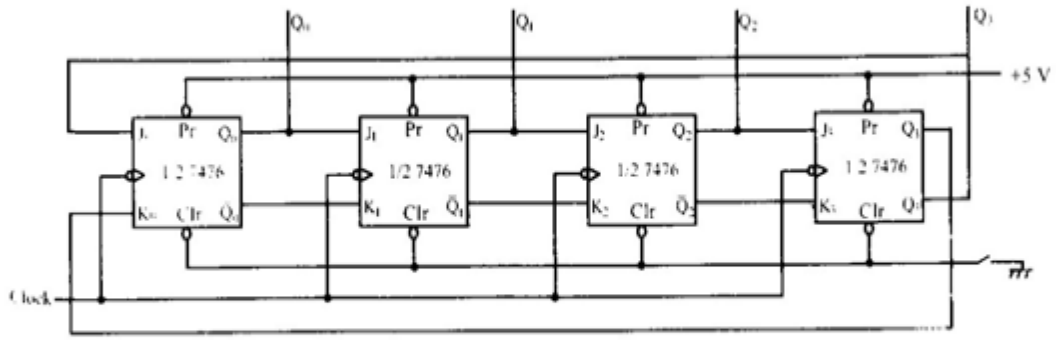
Clk	Q_0 Q_1 Q_2 Q_3
1	1 0 0 0
2	0 1 0 0
3	0 0 1 0
4	0 0 0 1

As it can be seen from the truth table there are four unique output stages for this counter. The modulus value of a ring counter is *n,* where *n* is the number of flip flops. Ring counter is called divided by N counter where N is the number of FF

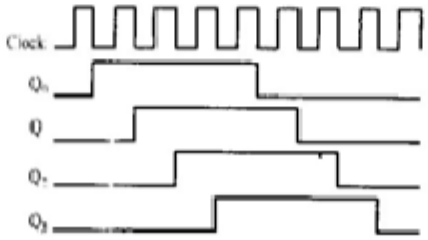
Johnson counter (Twisted ring counter)

The modulus value of a ring counter can be doubled by making a small change in the ring counter circuit. The Q' and Q of the last FFS are connected to the J and K input of the first FF respectively. This is the Johnson counter

Johnson counter



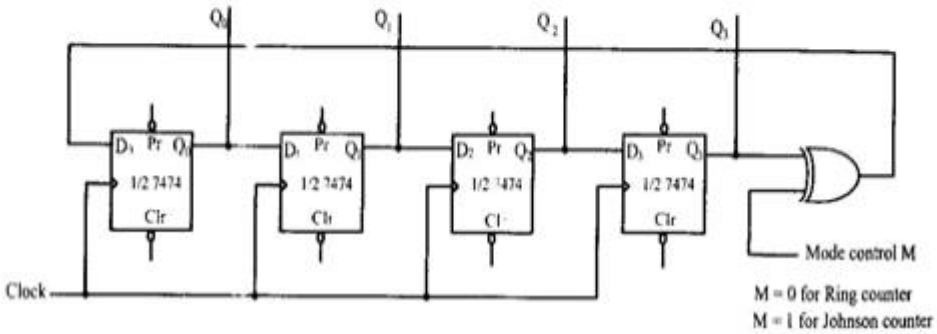
Waveforms for Johnson counter



Clk	Q_0 Q_1 Q_2 Q_3
0	0 0 0 0
1	1 0 0 0
2	1 1 0 0
3	1 1 1 0
4	1 1 1 1
5	0 1 1 1
6	0 0 1 1
7	0 0 0 1

Initially the FFs are reset. After first clock pulse FF0 is set and the remaining FFs are reset. After the eight clock pulse all the FFS are reset. There are eight different conditions creating a mode 8 Johnson counter. Johnson counter is called a twisted ring counter or divide by 2N counter

Ring/Johnson counter using mode control



PROCEDURE

1. Set up the ring counter and set clear Q outputs using PRESET and apply mono pulse.
2. Note down the state of the ring counter on the truth table for successive clock 0.
3. Repeat the steps for Johnsons counter

RESULT AND DISCUSSION

Four bit ring counter and the Johnson counter were set up using the JK FF and verified

EXPERIMENT NO : 10

CODE CONVERTER

AIM:

To design and implement a binary to gray and gray to binary converter.

Objective:

Theory:

The reflected binary code, also known as Gray code after Frank Gray, is a binary numeral system where two successive values differ in only one bit. The reflected binary code was originally designed to prevent spurious output from electromechanical switches. Today Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

Forming Gray Code:

The binary-reflected Gray code list for n bits can be generated recursively from the list for n-1 bits by reflecting the list (i.e. listing the entries in reverse order), concatenating the original list with the reversed list prefixing the entries in the original list with a binary 0, ang then prefixing the entries in the reflected list with a binary 1. For example, generating the n = 3 list from the n = 2 list:

Forming 1 bit to 2 bit gray code	Forming 2 bit to 3-bit gray code:
1-bit list: 0 1	Old 2-bit code: 00, 01, 11, 10
Reflect it: 10	New 2-bit code: 10, 11, 01, 00
Prefix old no. with 0: 00 01	Prefix old no. with 0: 000, 001, 011, 010
Prefix new no. with 1: 11 10	Prefix new no. with 1: 110, 111, 101, 100

Concatenate to get the 2-bit gray code: 00, 01, 11, 10	Concatenate both old and new no. 000, 001, 011, 010, 110, 111, 101, 100

Truth Table for Binary to Gray code converter

Decimal	Binary Input			Gray Output		
Decimal	**B2**	**B1**	**B0**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

Logical Equations:

G2	=	B2B1'B0' + B2B1'B1 + B2B1B0' + B2B1B0
G1	=	B2'B1B0' + B2'B1B0 + B2B1'B0' + B2B1'B0
G0	=	B2'B1'B0 + B2'B1B0' + B2B1'B0 + B2B1B0'

Simplification:

G2	=	B2B1'(B0' + B0) + B2B1(B0' + B0)
	=	B2B1' + B2B1
	=	B2(B1' +B1)
	=	B2
G1	=	B2'B1B0' + B2'B1B0 + B2B1'B0' + B2B1'B0
	=	B2'B1(B0' + B0) + B2B1'(B0' + B0)
	=	B2'B1 + B2B1'
	=	B2 XOR B1
G0	=	B2'B1'B0 + B2'B1B0' + B2B1'B0 + B2B1B0'
	=	B2'(B1'B0 + B1B0') + B2(B1'B0 + B1B0')
	=	(B1'B0 + B1B0') (B2' + B2)
	=	(B1'B0 + B1B0')
	=	B1 XOR B0

Logic Design:

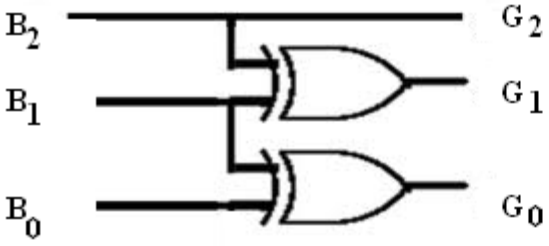
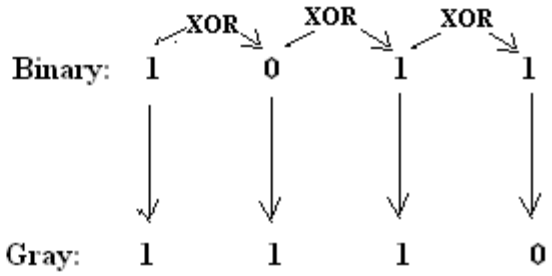


Fig: 3-bit Binary to Gray code Converter



Short Cut Binary to Gray code

Gray to Binary Code Converter

Truth Table for Binary to Gray code converter

Decimal	Gray Input				Binary Output		
Decimal	G2	G1	G0		B2	B1	B0
0	0	0	0		0	0	0
1	0	0	1		0	0	1
2	0	1	0		0	1	1
3	0	1	1		0	1	0
4	1	0	0		1	1	0
5	1	0	1		1	1	1
6	1	1	0		1	0	1
7	1	1	1		1	0	0

Logic Equations:

B2	=	G2G1G0' + G2G1G0 + G2G1'G0 + G2G1'G0'
B1	=	G2'G1G0 + G2'G1G0' + G2G1'G0 + G2G1'G0'
B0	=	G2'G1'G0 + G2'G1G0' + G2G1G0 + G2G1'G0'

Simplification:

B2	=	G2G1G0' + G2G1G0 + G2G1'G0 + G2G1'G0'
	=	G2G1(G0' + G0) + G2G1'(G0 + G0')
	=	G2G1 + G2G1'
	=	G2(G1+G1')
	=	G2
B1	=	G2'G1(G0 + G0') + G2G1'(G0 + G0')
	=	G2'G1 + G2G1'
	=	G2 XOR G1
B0	=	G2'G1'G0 + G2'G1G0' + G2G1G0 + G2G1'G0'
	=	G2'(G1'G0 + G1G0') + G2(G1G0 + G1'G0')
	=	G2'(G1 XOR G0) + G2(G1 XNOR G0) this is of the form A'B+AB'
	=	G2 XOR G1 XOR G0

Logic Diagram:

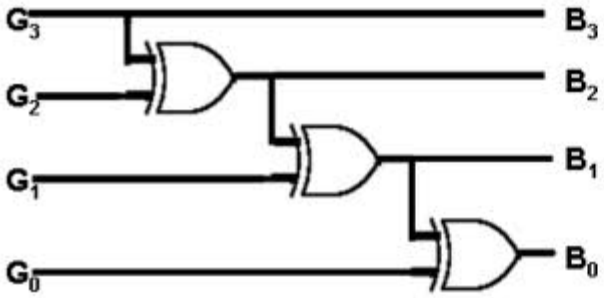
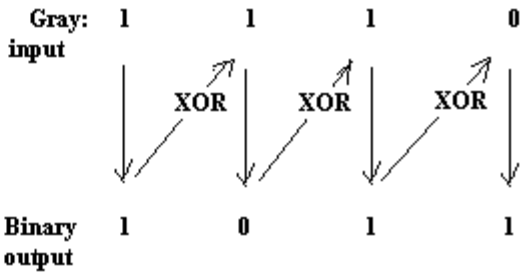


Fig: 3-bit Gray to Binary code converter



Short Cut Gray to Binary

Requirement:

IC 7486 01, LED 03 Resistors 220 Ohm 03, Power Supply, loose wire

Precaution:

- Use Proper power supply both rating and polarity
- Make correct connection on IC for the input and output
- Use diode with proper polarity, anode to + and cathod to ground
- Ensure power supply is switched off while making connection

Preparation:

- Keep a IC pin diagram with you for proper usage of the IC 7486
- Insert IC 7486 in the Bread board slots
- Make connection as per logic diagram

RESULT:

The circuit is tested and verified with the truth table